Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-85 (Cancelled)

86. (New) A radio comprising:

a first integrated circuit for receiving an RF signal and converting the RF signal to a baseband signal, and for converting the baseband signal to a serial digital signal using a one-bit sigma delta modulator for output, without a data rate clock signal, to a second integrated circuit; and

the second integrated circuit having a digital signal processor for receiving the serial digital signal output of the first integrated circuit, reconstructing the data rate clock, and recovering digital data in the received RF signal.

87. (New) The radio of claim 86 wherein the first integrated circuit converts the RF signal to I and Q baseband signals and converts both the I and Q baseband signals to I and Q serial digital signals for output, without a data rate clock signal, to the second integrated circuit, and the second integrated is configured to receive the I and Q serial digital signal outputs of the first integrated circuit, reconstruct the data rate clock and recover received I and Q digital data in the RF signal by the digital signal processor.

88. (New) The radio of claim 87 wherein the I and Q digital signals are coupled from the first integrated circuit to the second integrated circuit using low voltage differential coupling.

89. (New) The radio of claim 86 wherein the sigma delta modulator is controlled by a data rate clock, the data rate clock being programmable to provide various data rates in the serial digital signal for operation in various wireless communication systems.

90. (New) The radio of claim 86 wherein the second integrated circuit is also configured to convert digital data to be transmitted into a serial digital signal using a single bit sigma delta modulator for output, without a data rate clock signal, to the first integrated circuit, and the first integrated circuit is configured to receive the serial digital signal output of the first integrated circuit, to recover the digital data to be transmitted and modulate the digital data for RF transmission.

91. (New) A radio comprising:

a first integrated circuit for receiving an RF signal and converting the RF signal to I and Q baseband signals, and for converting the baseband signals to serial digital signals using one-bit sigma delta modulators for output, without a data rate clock signal, to a second integrated circuit; and

the second integrated circuit having a digital signal processor for receiving the serial digital signal outputs of the first integrated circuit, reconstructing the data rate clock, and recovering I and Q digital data in the received RF signal by the digital signal processor;

the sigma delta modulators being controlled by a data rate clock, the data rate clock being programmable to provide various data rates in the serial digital signals for operation in various wireless communication systems.

92. (New) The radio of claim 91 wherein the I and Q digital signals are coupled from the first integrated circuit to the second integrated circuit using low voltage differential coupling.

93. (New) The radio of claim 91 wherein the second integrated circuit is also configured to convert I and Q digital data to be transmitted into a serial digital signal using single bit sigma delta modulators for output, without a data rate clock signal, to the first integrated circuit, and the first integrated circuit is configured to receive the I and Q serial digital signal outputs of the first integrated circuit, recover the I and Q digital data to be transmitted and modulate and combine the modulated I and Q digital data for RF transmission.

94. (New) A radio comprising:

a first integrated circuit for receiving an RF signal and converting the RF signal to I and Q baseband signals, and for converting the baseband signals to serial digital signals using one-bit sigma delta modulators for output, without a data rate clock signal, to a second integrated circuit using low voltage differential coupling; and

the second integrated circuit having a digital signal processor for receiving the serial digital signal outputs of the first integrated circuit, reconstructing the data rate clock, and recovering I and Q digital data in the received RF signal by the digital signal processor;

the sigma delta modulators being controlled by a data rate clock, the data rate clock being programmable to provide various data rates in the serial digital signals for operation in various wireless communication systems;

the second integrated circuit also for converting I and Q digital data to be transmitted into a serial digital signal using single bit sigma delta modulators for output, without a data rate clock signal, to the first integrated circuit using low voltage differential coupling, and the first integrated circuit being configured to receive the I and Q serial digital signal outputs of the first integrated circuit, recover I and Q digital data to be transmitted and modulate and combine the I and Q modulated digital data for RF transmission.